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Low Power SRAM Memory System using Low Leak Asymmertic SRAM Cell

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***Abstract*— SRAM memory is an essential building block for almost all processors and VLSI (Very Large Scale Integration) systems which have data storage and data transfer capabilities. It also accounts for large space in VLSI circuits and has major share in the power consumption of Integrated Circuits (IC). This work presents a new 7T asymmetric SRAM cell, to address reduction in total power consumption and leakage power reduction in asymmetric 5T SRAM cell, during active mode of operation. The existing 5T SRAM has lesser total power consumption as compared to 6T SRAM cell, but has higher static power consumption. A novel leakage power reduction technique is applied to this asymmetric 5T SRAM cell to reduce its power during active write operation and as well total power consumption. A pair of NMOS and PMOS transistors in the ground path is used to achieve low leakage operation for this asymmetric SRAM cell. This SRAM cell uses one word-line, one bit-line and one read-line control. The functional blocks are bit cell, data write circuitry and sense amplifier. A complete memory system for data-write and data-read operations for a newly developed 7T SRAM cell is designed and simulation is carried out to verify the functionality, using cadence tool in 90nm GPDK process. Simulation carried out at supply voltage of 1.1V, indicate substantial power reduction in active mode for write '0' and total power consumption when compared to 6T SRAM cell and 5T SRAM cell. Data retention as well as access time is compared with existing 6T and 5T SRAM cells.**

***Keywords*- Static Power, Total Power, Static Random Access Memory(SRAM), Access Time, Asymmetric SRAM.**

I. Introduction

Large data storage circuitry is one of the primary concerns of a VLSI system. The demand for this has driven the memory development and fabrication technology towards higher storage densities and more compact design rules. More than half of the transistors in today's high-performance micro-processors are devoted to cache memories. The SRAM which functions as cache for the System on Chip (SOC) is a vital component in electronic systems. SRAM comprises a significant percentage of the total area and total power for many VLSI chips. Power consumption, stability and performance happen to be of great concern in the SRAM cell design.

Conventional 6-transistor SRAM (6T SRAM) consumes large power and has fairly large write and read access times. A 5T asymmetric SRAM suggested in [1], to reduce the cell area with performance and power consumption improvement. The ref. [1] suggests this 5T asymmetric cell, to exploit the overwhelming majority of write and read accesses which have a strong bias towards data bit '0'. This cell makes use of a single bitline unlike the dual bitline architecture of 6T SRAM cell. The power consumption in both writing '0' and '1' are same in case of 6T SRAM, because one of the bit-lines must be discharged low regardless of the written value [2]. The differential read bit-line is used during read operation and this necessitates one of the bitlines to be discharged irrespective of stored value [3]. Thus in conventional SRAM cell high dynamic energy consumption takes place due to the transitions on bit-lines in both writing '0' as well as reading '0'.

Both Read SNM and SRAM cell current values are highly dependent on the driving capability of the access NMOS transistor: Read SNM decreases with increases in driving capability, while SRAM cell current increases [4]. That is, the dependence of the two is in an inverse correlation [4]. Thus in conventional SRAM cell the read SNM of cell and cell current cannot adjust separately. A 5T SRAM cell is proposed in [1] to avoid inverse correlation between SRAM cell current and read SNM. This cell is based on loop-cutting strategy.

The 5T SRAM cell though achieves lesser total power dissipation, has static power dissipation which is quite significant. This static power dissipation is addressed in this work by introducing a novel leakage power reduction technique in the ground path of 5T SRAM cell, resulting in new 7T SRAM cell. A complete memory system is designed using this low power 7T asymmetric SRAM cell for single bit operation, which comprises of Write Circuit- to enable writing of data bit in to the cell, when enabled by write enable (WE), signal, Column Select Circuit, activated by signal Ymux, to select the memory for reading, and Read Circuit- which generates two complementary output signals READ and READ_BAR, when enabled by sense enable (SAE), signal. The static power consumption while writing '0' and '1', for conventional 6T SRAM cell, 5T SRAM cell and new low power 7T SRAM cell are measured and compared using cadence design tools. The total power consumption of these three cells is also compared.

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II. Literature Review

Due to the on-going technology scaling the supply voltage gets scaled which in-turn scales down the threshold voltage, channel length and gate oxide thickness. This increases the leakage currents and hence leakage power in VLSI circuits. For low power applications reducing leakage power has become an utmost priority [5].

For more than 30 years, CMOS devices are scaled to achieve higher density and performance and lower power consumption. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years. Supply voltage has been scaled down in order to keep the power consumption under control. Hence, the transistor threshold voltage has to be commensurately scaled to maintain a high drive current and achieve performance improvement. However, the threshold voltage scaling results in the substantial increase of the sub-threshold leakage current [5].

Previously many different SRAM topologies have been developed to cater to the need of reliable Sub-threshold applications. Low leakage asymmetric cells that reduce sub threshold leakage currents were proposed by N.Azizi etal., [6,7]. These cells exploit the fact that most of the bits stored in caches are zeroes.

The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using SRAM cells. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation [8]. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines [9-11]. Especially for modern VLSI processor design, SRAM takes large part of power consumption portion and area overhead [12].

III. Operation And Design Constraints Of 5t Sram Cell

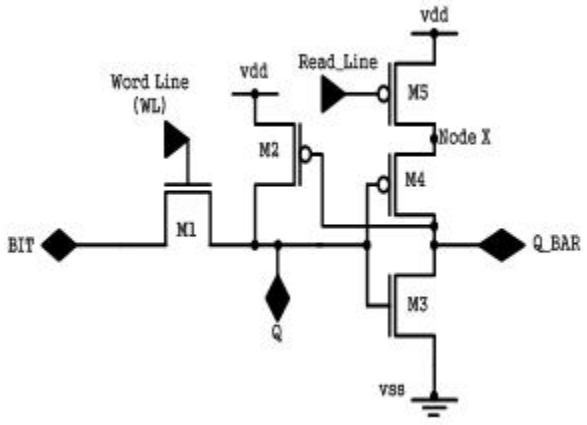

Figure 1. 5t Sram Cell

5T SRAM cell is as shown in the fig. 1. 5T SRAM cell has one bit-line, one word-line and one read-line control signal [1]. The cell has one Access transistors (M1), one Drive transistors (M3), one Load transistor (M4), one Feedback-cutting transistor (M5) and another load transistor (M2) that forms a positive feedback path with M3.

A. Operation Of Cell

During idle mode of cell (WL=0 and Read_Line=0, write and read operation is not performed on cell); M1 is OFF, the transistor M5 is ON and M5 pulls node X to V_{DD}. When '1' stored in cell, M3 and M2 are ON and there is a positive feedback between nodes Q and Q_BAR therefore Q is pulled to VDD by M2 and Q_BAR pulled to V_{SS} by M3. When '0' is stored in cell, M4 is ON and since node X maintained at V_{DD} by M5, Q_BAR is pulled to V_{DD}, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied [1].

$$I_{DS(M1)} > I_{SD(M2)} + I_{gate(M3)} + I_{gate(M4)}$$

In active mode, for WRITE 1 operation, WL=1, Read_Line=0 and BIT=1. The transistor M1 is ON and it transmits data present on B which makes Q=1, and therefore M3 is ON, and therefore Q_BAR=0. Similarly while writing logic '0', the node BIT=0 which makes Q=0, and therefore M4 is ON which makes Q_BAR=1[1].

IV. Proposed 7T SRAM

The write data of the benchmark programs have an overwhelming majority of the write bits '0' [ref 1 of 2009 paper]. Based on this observation, a novel leakage reduction technique is applied to existing 5T SRAM cell and a new 7T SRAM cell is developed, which drastically reduces the SRAM power dissipated in writing '0' and also reduces the total power dissipation. The most important characteristics of the 7T cell are summarized as follows. First, in the conventional SRAM cell, because one of two bitlines must be discharged to low regardless of written value, the power consumption in both writing '0' and '1' are the same. In contrast, the 7T cell uses the complement of input data to perform the write operation that prevents the single write bitline from being discharged if the written value is '0'. Therefore, the write '0' power is far less than the write '1' power in the 7T cell. Second, writing cell state from low to high is considerably more difficult in single-bitline configuration because it presents conditions similar to that of the read mode. In 7T cell, writing cell state from low to high is easily achieved by the positive feedback.

The 5T SRAM cell shown in fig. 1 consumes more power during write '0' and has more total power consumption. In order to reduce this power consumption a pair of NMOS-PMOS transistors is used in the ground path as shown in fig. 2. The NMOS M6 transistor is driven by storage node Q while the PMOS M7 transistor is driven by storage node Q-BAR. This 7T SRAM cell has substantially less static power consumption during active write '0', and less total power dissipation. The newly developed 7T SRAM cell reduces the power consumption during active state and total power in the SRAM cell compared to 6T and 5T SRAM cell by increasing the resistance of ground path and reducing the

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current.

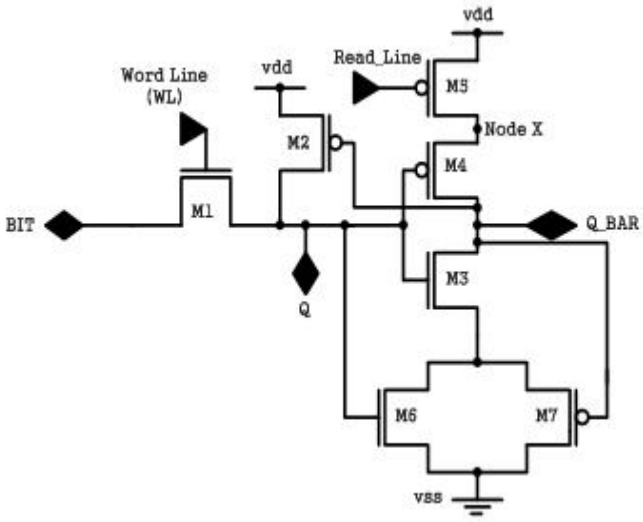

Figure 2. 7T SRAM Cell

A. Write Operation

During writing data '1', Read_Line is maintained at ground. Feedback cutting transistor M5 is ON and the node X is pulled to V_{DD} by M5. The data bit '1' will be driven onto the 'BIT' and the 'WL' is asserted to V_{DD}. The node 'Q' will be pulled up to V_{DD}-V_{THN} by the NMOS transistor M1. This causes the driver transistors M3 to be ON and node Q_BAR will be pulled down to ground. The load transistor M2 becomes ON and maintains the node Q at the level V_{DD}.

While writing data '0', the node Q is pulled down to ground by NMOS access transistor M1, which causes M4 to be ON and node Q_BAR to be pulled up to V_{DD}. During idle mode, word-line and bit-line are asserted to logic low state.

The effect of new leakage reduction circuit comprising of transistors M6 and M7 is to increase the resistance of ground path and reduce the current. While writing '1', Q=1 and it causes the transistor M6 to be ON along with transistor M3. Node Q_BAR is'0' and it causes the transistor M7 to be ON. This introduces a resistive path in series with transistor M3 and causes the drain-to-source current of M3 to reduce and hence lower static power dissipation.

While writing a '0', M3 is OFF, M6 is OFF and M7 is also OFF. There is a large resistive path comprising of off-resistances of M6 and M7 in series with M3 and this reduces the leakage current flowing to the ground through the OFF transistors M3. Due to the stack property for more than one OFF transistors in a series path of transistors, the leakage current comes down. The static power dissipation for write '0' has come down drastically.

B. Read Operation

Consider the read circuitry in fig. 4. Positive pulse is applied to Ymux control signal this causes the Ymux transistor to be ON and discharge the 'BIT' to ground state and then it is made to float. The Read_Line is maintained at V_{DD} and transistor M5 is OFF. The WL is activated to logic '1' state. If stored value is '1', the node Q is at logic high level and causes the 'BIT' to be pulled up to high state by transistor M1. On the other hand, if stored value is '0', the node Q causes 'BIT' to be driven to '0' state so that the voltage of bit-line and Q node are equalized. Now the WL will be deactivated and read signal is returned to ground and the sense amplifier is turned on to read the data on the bit-line.

V. 7T Asymmetric SRAM Memory System For Single Bit Write And Read Operation

The single bit memory system comprising of SRAM cell, write circuit and sense amplifier is designed and simulated in 90nm technology. The complete setup for data write and read for single bit memory system is shown in fig. 3 and schematic in fig. 4. This block diagram shows all the different peripheral circuits with all input signals: Write Enable, Data bit, Word Line and Sense Amplifier Enable combined with the SRAM cell to form a complete working SRAM system for write and read operation. The simulation results for writing and reading data bits '0' and '1' with data retention are shown in fig. 5 and in fig. 6 respectively.

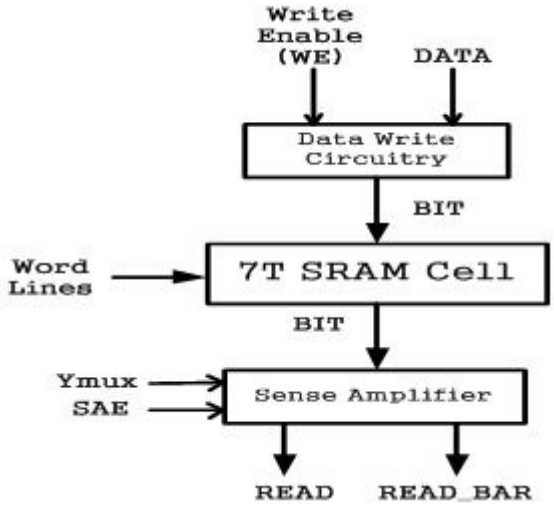

Figure 3. Block diagram of 7T SRAM system

A. Write Circuitry

The write circuit is used to write the data into the cell. The write circuit is enabled by the Write Enable (WE) signal and drives the bit-line. The input data is written into the cell only when WE signal is high; else the data is not passed onto the cell. Fig. 4 shows the schematic of write circuit.

B. Sense Amplifier

The function of sense amplifier is to read the data from the cell. The sense amplifier circuit is active during the read operation only. Fig. 4 shows the single-ended sense amplifier that is used for reading the data from 7T SRAM cell [1].

During reading, the write circuit is disabled or WE=0, M5 is OFF and WL=1. When the data stored in cell is '1' i.e. Q=1 and Q_BAR=0, the voltage of bit line is pulled to high voltage by M1 which is sensed by the sense amplifier resulting in READ=1 and READ_BAR=0. Similarly when '0' in cell Q=0

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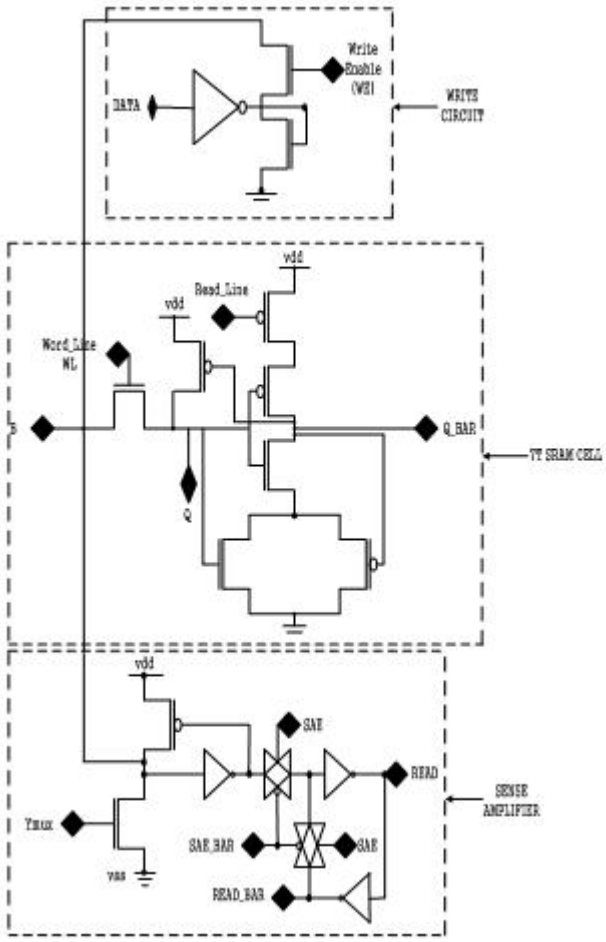

Figure 4. Memory System for 7T SRAM system

and Q_BAR=1, the voltage of bit line and Q equalized resulting in READ=0 and READ_BAR=1.

VI. Simulation Results

The simulation results for the 6T SRAM cell, 5T SRAM cell and low leak 7T SRAM cell without and with peripheral circuitry are presented in this section. The static power dissipation is measured both during memory active and inactive states by holding WL and BIT at appropriate voltage levels. To measure Static Power Dissipation during write '1' operation, the different control signals are maintained as WL=1, Read_Line=0, and BIT=1. For write '0' operation with WL=1, Read_Line=0, and BIT=0 are maintained. The Static Power Dissipation during inactive state of operation is measured by maintaining WL=BIT=0, and Read_Line=1.

When compared to the static power dissipation during write '1' and write '0' with conventional 6T SRAM cell, it is observed that for the Novel new 7T SRAM cell 27X times reduction is observed for both write '1' and write '0'. In comparison with 5T SRAM cell for write '1' operation the static power is almost same but for write '0' it is reduced considerably by 20X times. The static power dissipation during retention mode when compared with single bit conventional 6T SRAM cell, it is observed that for both 5T SRAM cell and Novel 7T SRAM cell the static power is slightly more. Access time is measured for 6T, 5T, and 7T SRAM cell. Results show that among the three cells 7T SRAM cell has more access time. Also the total power dissipation of 7T SRAM cell is reduced by 7X times for 6T SRAM cell and by 3X times for 5T SRAM cell. A comparison of the Access Time, Static and Total Power Dissipation in the Novel 7T SRAM cell with conventional 6T SRAM cell and existing 5T SRAM cell are presented in Table I.

Access Time during write and read is measured for single bit read/write memory system for 6T SRAM and New 7T SRAM. The total power dissipation is also measured. The results are given in Table II. The results show that for 7T, the write access time is slightly more compared to 6T but the total power consumption is reduced by 6X times.

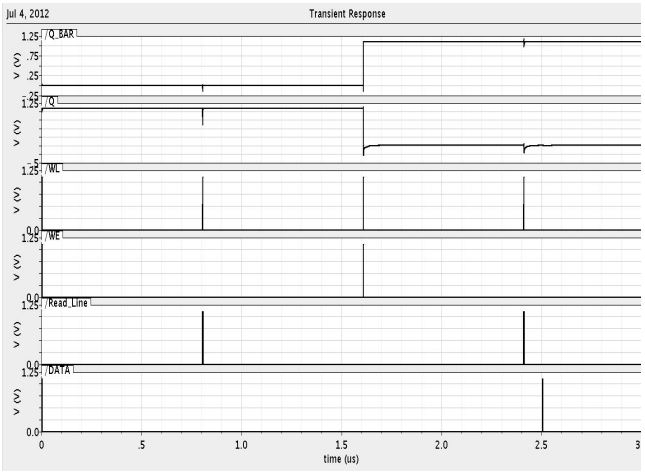

Figure 5.Simulation results for single bit 7T SRAM memory system for writing data bits '0' and '1' with data retention

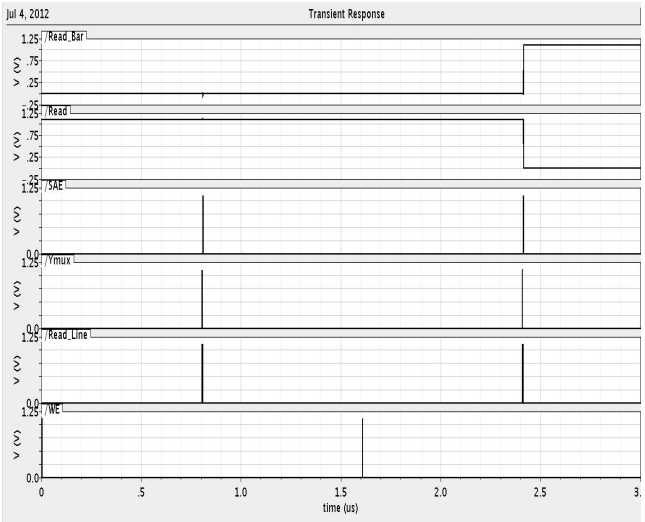

Figure 6. Simulation results for single bit 7T SRAM memory system for reading data bits '0' and '1' with data retention

VII. Conclusion

In this paper, a 7T SRAM cell with novel leakage reduction technique that consists of pair of NMOS-PMOS transistor in the ground path is proposed. Simulation results show that, the 7T SRAM cell has significant reduction in static power dissipation for write '0' operation by a factor of 27X times

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TABLE I. STATIC POWER, TOTAL POWER AND ACCESS TIME FOR SINGLE SRAM CELL FOR V_{DD}=1.1V

SRAM cell	Static power (nW)			Total power (nW)	Access time (psec)
	For write '1'	*For write '0'*	*Retention mode*		
Conventional 6T SRAM cell	67.542	67.542	67.601	115.5	38.9014
Existing 5T SRAM cell	2.071	45.670	73.255	42.78	21.8995
New 7T SRAM cell	2.544	2.315	73.727	17.08	41.5543

TABLE II. ACCESS TIME AND TOTAL POWER DISSIPATION FOR SINGLE BIT SRAM SYSTEM FOR V_{DD}=1.1V

Single Bit SRAM system	Write access time (psec)	Total power dissipation (nW)
Conventional 6T SRAM system	36.064	682.2
7T SRAM system	81.619	113.7

when compared to conventional 6T SRAM cell and by 20X times reduction in static power for write '0' when compared to 5T SRAM cell. For write '1' operation, the static power dissipation of 7T SRAM cell has 27X times reduction compared to 6T SRAM cell. The total power is also reduced by a factor of 7X times when compared to 6T SRAM cell and by 3X times when compared to 5T SRAM cell. The power dissipation in the SRAM during active mode is addressed in this cell effectively along with significant reduction in static power dissipation with better stability but with little area overhead.

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